REMARKS

Claims 1-20 are pending in the current application. Of those, claims 1, 7, 10, and 20 are independent claims. Claims 1-3, 7-9, 10, and 20 are amended by this Response. No claims are canceled or added by this Response.

Claim Rejections under 35 U.S.C. § 112

Claims 1-20 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Applicant respectfully traverses this rejection.

In regards to claims 1-5 and 7-20, the Examiner asserts it is unclear if the peripheral device is within the processor as shown in figure 1 and 2 of the drawings as well as mentioned throughout the specification. In regards to claim 6, the Examiner asserts it is uncertain how the processor can have at least one of a wireless LAN card, a PC or PCMIA card, and a liquid crystal display (LCD) within the processor.

Applicant recognizes that the specification defines a processor 200 as including "a control circuit 210, a multiplexer [] 250, a processor core 260, and a peripheral device 270." However, Applicant respectfully submits that one skilled in the art would clearly recognize that the processor 200 may not be a "processor" in the more traditional sense of the word. In particular, Applicant notes that the processor 200 in example embodiments may contain a processor core 260. Further, Applicant notes, as the Examiner recognized, that the processor 200 in example embodiments may include a peripheral device 270, wherein the pheriherial device may be wireless LAN card, a PC or PCMIA card, and/or a liquid crystal display (LCD).

MPEP 2173.05(a) III states "consistent with the well-established axiom in patent law that a patentee or applicant is free to be his or her own lexicographer, a patentee or applicant may use terms in a manner contrary to or inconsistent with one or more of their ordinary meanings if the

written description clearly redefines the terms." See, e.g., *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999).

Applicant respectfully submits that one skilled in the art would recognize from the decription of the processor 200 in example embodiments in the specification, in particular, the inclusion of a processor core and/or a peripheral device within the processor 200, that a processor according to example embodiments may be interpreted more broadly than what the Examiner might consider a more traditional definition of a processor. For example, Applicant notes that the processor 200 in example embodiments may be more properly characterized as a "processor system" or "processor block," and that the inclusion of only the terms "the processor 200" may be a translation problem encountered in translating the priority document from Korean to English. Accordingly, Applicant respectfully submits that one skilled in the art would recognize that the peripheral device may be included in the processor (e.g., along with a processor core), and therefore, how example embodiments may have at least one of a wireless LAN card, a PC or PCMIA card, and a liquid crystal display (LCD) within the processor. Applicant notes that should the Examiner feel the specification would be more clear if "the processor 200" is defined as "the processor system 200" or "the processor block 200," Applicant would be willing to consider amending the specification to include such clarifying language.

In view of the above, Applicant respectfully requests the rejections under 35 U.S.C. § 112, first paragraph, be withdrawn.

Claim Rejections under 35 U.S.C. § 103

Claims 1-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim (U.S. Pub. No. 2002/0026596, herein Kim) in view of Tam et al. (U.S. Pat. No. 6,608,528, herein Kim). Applicant respectfully traverses this rejection.

Claim 1 is amended to recite *inter alia* "a selecting circuit for determining at least one of operation states and operating frequencies of a high-speed control circuit and a low-speed and low-power control circuit and for outputting a selection signal based on the determination."

Kim discloses at paragraph [0017] "The clock selection unit 140 outputs a selection signal for outputting one of the first and second clock signal CLOCK1 and CLOCK2 as the processor clock signal P_CLOCK, in response to a control signal that is outputted from the instruction decoder 150." Therefore, Kim clearly does not disclose "a selecting circuit for determining at least one of operation states and operating frequencies of a high-speed control circuit and a low-speed and low-power control circuit and for outputting a selection signal based on the determination" as required by claim 1.

Tam discloses at col. 9, lines 34-41 "The frequency/voltage control logic 342 analyzes input from sensors that can track current, power, temperature, or processing load. The sensor values are evaluated to determine how much power the processor 300 is consuming. [b]ased on what the processor power consumption is, the controller 342 can find an appropriate operating point for the processor 300." Therefore, Tam clearly does not disclose "a selecting circuit for determining at least one of operation states and operating frequencies of a high-speed control circuit and a low-speed and low-power control circuit and for outputting a selection signal based on the determination" as required by claim 1. To the contrary, Tam only analyzes the processor 300, and does not determine operation states and/or operating frequencies of a high-speed control circuit and a low-speed and low-power control circuit. Further, Tam is concerned only with processor power consumption, Tam does not determine operation states or operating frequency, let alone make a determination and/or output a selection signal based on operation states or operating frequency.

Accordingly, Applicant respectfully submits that even assuming for the sake of argument Kim and Tam are properly combinable (which Applicant does not admit), both Kim and Tam, either alone or in combination, fail to disclose "a selecting circuit for determining at least one of operation states and operating frequencies of a high-speed control circuit and a low-speed and low-power control circuit and for outputting a selection signal based on the determination" as required by claim 1. Therefore, claim 1 is patentable for at least the above reasons. Further, claims 7, 10, and 20 contain features somewhat similar to those discussed above in regards to claim 1, and therefore, claims 7, 10, and 20 are patentable for at least somewhat similar reasons as claim 1. Claims 2-6, 8-9, and 11-29, which depend from one of claims 1, 7, and 10, are patentable for at least the same reasons as claim 1 as well as on their own merits.

In view of the above, Applicant respectfully requests the rejections under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of the claims in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____

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